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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/664,910	Applicant(s) HALBERT ET AL.
	Examiner Dipakkumar Gandhi	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8,10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

1. Applicants' request for reconsideration filed on 4/22/2003 has been reviewed.

2. Amendment A filed on 4/22/2003 has been entered.

3. Applicants' arguments with respect to claims 1-53 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 2, 7, 8, 16, 17, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1) in view of Bates et al. (US 6,477,674 B1), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1).

As per claim 1, Gillingham teaches a memory component and built-in self test (col. 2, lines 44-46, Gillingham), comprising:

An input/output interface coupled to the memory array and having a loopback (DRAM 38, data-in, data-out, data line 34 in figure 2, col. 2, lines 55-57, Gillingham) and

A controller (abstract, Gillingham).

The Examiner would like to point out that the compare register and the controller may be embodied within a single device or a common circuit (page 6, lines 12-13, specification of the present invention).

However Gillingham does not explicitly teach the specific use of a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface.

Bates et al., in an analogous art, teach that I/O loopback tests are typically carried out by providing data from a functional logic block (or FLB) within the IC (e.g. a microprocessor), and driving the data out through the output component of each I/O buffer (i.e. input/output interface). Subsequently, the data is driven back through the input component of the I/O buffer to the FLB in order to verify that the correct data has been received. Consequently, the IC verifies whether the input and output components of each I/O buffer is functioning properly (col. 1, lines 33-41, Bates et al.). The Examiner would like to point out that the functional logic block includes a controller and a compare register.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gillingham's patent with the teachings of Bates et al. by including an additional step of using a controller to transmit input/output test data to the input/output interface, and to receive the input/output test data from the loopback of the input/output interface; and a compare register to compare the input/output test data transmitted to the input/output interface with the input/output test data received from the input/output interface.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify the proper functionality and timing of components within the input/output interface of a memory component.

Gillingham also does not teach a memory component with built-in self test (Gillingham teaches that the BIST controller is external of the memory module that contains the memory component, DRAM).

However Cloud et al. in an analogous art teach that the memory device 10 is a SDRAM and the memory module 12 may also include a BIST circuit 73 for testing the circuitry on the module 12 (figure 6, col. 6, lines 12-13, lines 33-34, Cloud et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gillingham's patent with the teachings of Cloud et al. by including an additional step of using a memory component with built-in self-test.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a memory component with built-in self-test would provide the opportunity to independently test a memory component without affecting other circuits.

Gillingham also does not teach that the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

However Ryan in an analogous art teaches that each memory module 320 has at least one pipelined memory subsystem. For purposes of illustration, memory module 320.1 is shown with a single pipelined memory subsystem 330. Memory subsystem 330 comprises C/A buffer register 331, a plurality M of memory devices 335 and a data buffer 341. C/A buffer register 331 is coupled between C/A bus 310 and the plurality M of memory devices 335.1 through 335.M. C/A buffer register 331 receives and latches the command and address information from C/A bus 310. Data register 341 is connected between data bus 315 and the plurality M of memory modules 335. For memory read operations, data register 341 receives and latches data information from the plurality of memory devices 335 and drives the data information to data bus 320. For memory write operations, data register 341 receives and latches data information from data bus 320 and drives the data information to the plurality of memory devices (figure 3, col. 7, lines 29-45, Ryan).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gillingham's patent with the teachings of Ryan by including an additional step of using the memory component residing within a memory module having a plurality of memory devices and at least one buffer.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the memory component

residing within a memory module having a plurality of memory devices and at least one buffer would provide the opportunity to provide a memory system with large data storage capacity.

- As per claim 2, Gillingham, Bates et al., Cloud et al. and Ryan teach the additional limitations. Gillingham teaches that the memory component is a dynamic random access memory, DRAM (col. 2, lines 44-45, Gillingham).
- As per claim 7, Gillingham, Bates et al., Cloud et al. and Ryan teach the additional limitations. Bates et al. teach the memory component wherein the compare register generates a test result based on the input/output test data transmitted to the input/output interface compared with the input/output test data received from the input/output interface (col. 1, lines 33-39, Bates et al.). The Examiner would like to point out that the functional logic block includes a controller and a compare register.
- As per claim 8, Gillingham, Bates et al., Cloud et al. and Ryan teach the additional limitations. Gillingham teaches the memory component wherein the controller is adapted to transmit memory array test data to a memory array to store the test data therein, and to read the memory array test data from the memory array, and the compare register is adapted to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array (controller 23, DRAM 38, data-in and data-out in figure 2, col. 2, lines 49-57, Gillingham). The Examiner would like to point out that the compare register and the controller may be embodied within a single device or a common circuit (page 6, lines 12-13, specification of the present invention).
- As per claim 16 (method), it follows the same limitations as claim 1 (memory component). Claim 16 is also rejected under the same rationale as set forth in the claim 1 (as rejected above).
- As per claim 17 (method), it follows the same limitations as claim 2 (memory component). Claim 17 is also rejected under the same rationale as set forth in the claim 2 (as rejected above).
- As per claim 22 (method), it follows the same limitations as claim 7 (memory component). Claim 22 is also rejected under the same rationale as set forth in the claim 7 (as rejected above).
- As per claim 23 (method), it follows the same limitations as claim 8 (memory component). Claim 23 is also rejected under the same rationale as set forth in the claim 8 (as rejected above).

7. Claims 3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Bates et al. (US 6,477,674 B1), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1) as applied to claim 1 above, and further in view of Krick et al. (US 5,638,382). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

8. Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Bates et al. (US 6,477,674 B1), Cloud et al. (US 5,815,427), Ryan (US 6,247,070 B1) and Krick et al. (US 5,638,382) as applied to claim 3 above, and further in view of McAlpine (US 4,837,785). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

9. Claims 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Bates et al. (US 6,477,674 B1), Cloud et al. (US 5,815,427), Ryan (US 6,247,070 B1) and Krick et al. (US 5,638,382) as applied to claim 3 above, and further in view of Emkell et al. (US 5,633,878). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

10. Claims 6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Bates et al. (US 6,477,674 B1), Cloud et al. (US 5,815,427), Ryan (US 6,247,070 B1) and Krick et al. (US 5,638,382) as applied to claim 3 above, and further in view of Tomioka et al. (US 5,835,936). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

11. Claims 9, 10, 15, 24, 25 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1) in view of Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1).

As per claim 9, Gillingham teaches a memory component and a built-in self test (col. 2, lines 44-46, Gillingham), comprising:

A memory array (col. 2, line 51, Gillingham);

An input/output interface coupled to the memory array and having a loopback (DRAM 38, data-in, data-out, data line 34 in figure 2, col. 2, lines 55-57, Gillingham);

A controller to transmit memory array test data to the memory array to store the memory array test data, and to read the memory array test data from the memory array and a compare register to compare the memory array test data transmitted to the memory array with the memory array test data read from the memory array (controller 23, DRAM 38, data-in and data-out in figure 2, col. 2, lines 49-57, Gillingham).

The Examiner would like to point out that the compare register and the controller may be embodied within a single device or a common circuit (page 6, lines 12-13, specification of the present invention).

However Gillingham does not teach a memory component with built-in self test (Gillingham teaches that the BIST controller is external of the memory module that contains the memory component, DRAM).

Cloud et al. in an analogous art teach that the memory device 10 is a SDRAM and the memory module 12 may also include a BIST circuit 73 for testing the circuitry on the module 12 (figure 6, col. 6, lines 12-13, lines 33-34, Cloud et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gillingham's patent with the teachings of Cloud et al. by including an additional step of using a memory component with built-in self-test.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a memory component with built-in self-test would provide the opportunity to independently test a memory component without affecting other circuits.

Gillingham also does not teach that the memory component resides within a memory module having a plurality of memory devices and at least one buffer.

However Ryan in an analogous art teaches that each memory module 320 has at least one pipelined memory subsystem. For purposes of illustration, memory module 320.1 is shown with a single pipelined memory subsystem 330. Memory subsystem 330 comprises C/A buffer register 331, a plurality M of memory devices 335 and a data buffer 341. C/A buffer register 331 is coupled between C/A bus 310 and the plurality M of memory devices 335.1 through 335.M. C/A buffer register 331 receives and latches the command and address information from C/A bus 310. Data register 341 is connected between data bus 315 and the plurality M of memory modules 335. For memory read operations, data register 341 receives and latches data information from the plurality of memory devices 335 and drives the data information to data bus 320. For memory write operations, data register 341 receives and latches data information from data bus 320 and drives the data information to the plurality of memory devices (figure 3, col. 7, lines 29-45, Ryan).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gillingham's patent with the teachings of Ryan by including an additional step of using the memory component residing within a memory module having a plurality of memory devices and at least one buffer.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the memory component residing within a memory module having a plurality of memory devices and at least one buffer would provide the opportunity to provide a memory system with large data storage capacity.

- As per claim 10, Gillingham, Cloud et al. and Ryan teach the additional limitations.

Gillingham teaches that the memory component is a dynamic random access memory, DRAM (col. 2, lines 44-45, Gillingham).

- As per claim 15, Gillingham, Cloud et al. and Ryan teach the additional limitations.

Gillingham teaches that the compare register generates a test result based on the memory array test data transmitted to the memory array compared with the memory array test data read from the memory array (col. 2, lines 52-55, col. 4, lines 46-47, Gillingham).

- As per claim 24, Gillingham, Cloud et al. and Ryan teach the additional limitations.

Gillingham teaches a method of testing a memory component and built-in self test (col. 2, lines 44-46, Gillingham), comprising:

Transmitting memory array test data to a memory array,

Storing the memory array test data in the memory array,

Reading the memory array test data from the memory array; and

Comparing the memory array test data transmitted to the memory array with the memory array test data read from the memory array (controller 23, DRAM 38, data-in and data-out in figure 2, col. 2, lines 49-57, Gillingham).

Cloud et al teach a memory component with built-in self test (figure 6, col. 6, lines 12-13, lines 33-34, Cloud et al.).

Ryan teaches that the memory component resides within a memory module having a plurality of memory devices and at least one buffer (figure 3, col. 7, lines 29-45, Ryan).

- As per claim 25, Gillingham, Cloud et al. and Ryan teach the additional limitations.

Gillingham teaches a method wherein the memory component is a dynamic random access memory, DRAM (col. 2, lines 44-45, Gillingham).

- As per claim 30, Gillingham, Cloud et al. and Ryan teach the additional limitations.

Gillingham teaches a method wherein the compare register generates a test result based on the memory array test data transmitted to the memory array compared with the memory array test data read from the memory array (col. 2, lines 52-55, col. 4, lines 46-47, Gillingham).

12. Claims 11 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Cloud et al. (US 5,815,427), Ryan (US 6,247,070 B1) as applied to claim 9 above, and further in view of Krick et al. (US 5,638,382). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

13. Claims 12 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Cloud et al. (US 5,815,427), Ryan (US 6,247,070 B1) and Krick et al. (US 5,638,382) as applied to claim 11 above, and further in view of McAlpine (US 4,837,785). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

14. Claims 13 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Cloud et al. (US 5,815,427), Ryan (US 6,247,070 B1) and Krick et al. (US 5,638,382) as applied to claim 11 above, and further in view of Ernkell et al. (US 5,633,878). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

15. Claims 14 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham (US 6,182,257 B1), Cloud et al. (US 5,815,427), Ryan (US 6,247,070 B1) and Krick et al. (US 5,638,382) as applied to claim 11 above, and further in view of Tomioka et al. (US 5,835,936). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

16. Claims 31, 32, 33, 36, 38, 39, 40, 41, 42, 45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 6,415,403 B1) in view of Osawa et al. (US 5,946,247), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1).

As per claim 31, Huang et al. teaches a built-in self test for memory (figure 1, col. 4, line 11, Huang et al.), comprising:

At least one memory component (DRAM 13 in figure 1, col. 4, line 13, Huang et al.);

An address and command buffer adapted to transmit address and command data and test data to at least one memory component (interface buffers 14 and DRAM 13 in figure 1, col. 4, lines 14-17, lines 26-29, Huang et al.); and

At least one data buffer to receive the test data from the address and command buffer, to receive the test data from at least one memory component, and to compare the test data received from the address and command buffer with the test data received from at least one memory component to generate the test result (col. 4, lines 14-18, lines 31-33, Huang et al.).

The Examiner would like to point out that the data buffers and the address and command buffer may be incorporated into a single buffer device (page 3, lines 20-21, specification of the present invention).

However Huang et al. do not explicitly teach the specific use of a register to receive a test result.

Osawa et al. in an analogous art, teach that the register circuit 706 receives the test result upon the RAM test by the self-test circuit 702 (figure 142, col. 77, lines 62-64, Osawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Osawa et al. by including an additional step of using a register to receive a test result.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a register to receive a test result would provide the opportunity to hold the test result in form of binary data.

Huang et al. also does not teach a memory module with built-in self-test.

However Cloud et al. in an analogous art teach that the memory device 10 is a SDRAM and the memory module 12 may also include a BIST circuit 73 for testing the circuitry on the module 12 (figure 6, col. 6, lines 12-13, lines 33-34, Cloud et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Cloud et al. by including an additional step of using a memory module with built-in self-test.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a memory module with built-in self-test would provide the opportunity to independently test a memory component without affecting other circuits.

Huang et al. also does not teach that the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module.

However Ryan in an analogous art teaches that each memory module 320 has at least one pipelined memory subsystem. For purposes of illustration, memory module 320.1 is shown with a single pipelined memory subsystem 330. Memory subsystem 330 comprises C/A buffer register 331, a plurality M of memory devices 335 and a data buffer 341. C/A buffer register 331 is coupled between C/A bus 310 and the plurality M of memory devices 335.1 through 335.M. C/A buffer register 331 receives and latches the command and address information from C/A bus 310. Data register 341 is connected between data bus 315 and the plurality M of memory modules 335. For memory read operations, data register 341 receives and latches data information from the plurality of memory devices 335 and drives the data information to data bus 320. For memory write operations, data register 341 receives and latches data information from data bus 320 and drives the data information to the plurality of memory devices (figure 3, col. 7, lines 29-45, Ryan).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Ryan by including an additional step of using the plurality of memory components, the address and command buffer, and the at least one data buffer all residing within the memory module.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the plurality of memory components, the address and command buffer, and the at least one data buffer all residing within the memory module would provide the opportunity to provide a memory system with large data storage capacity.

- As per claim 32, Huang et al., Osawa et al., Cloud et al., and Ryan teach the additional limitations. Huang et al. teach the memory module wherein the address and command buffer and the data buffer are within a single buffer chip (figure 1, col. 4, lines 10-14, Huang et al.).
- As per claim 33, Huang et al., Osawa et al., Cloud et al., and Ryan teach the additional limitations. Huang et al. teach the memory module wherein at least one memory component is a dynamic random access memory, DRAM (DRAM 13 in figure 1, col. 4, lines 13-14, Huang et al.).
- As per claim 36, Huang et al., Osawa et al., Cloud et al., and Ryan teach the additional limitations. Osawa et al. teach that the self-test circuit 702 includes a microcomputer 702a as shown in FIG. 143. A program stored in a ROM or a RAM (not shown) of the microcomputer 702a controls a self-test operation. In FIG. 143, a test pattern signal supplied to the RAM with test circuit 703 is indicated as "Test Pattern", figure 142, 143, col. 75, lines 54-57, 67, col. 76, lines 1-2, Osawa et al. (i.e. memory module, wherein the test data is obtained from a data bus through a memory controller).
- As per claim 38, Huang et al., Osawa et al., Cloud et al., and Ryan teach the additional limitations. Osawa et al. teach that FIG. 1 is a logic circuit diagram showing a semiconductor memory (RAM) testing device. The comparison circuit 232 is formed by a single exclusive OR circuit (hereinafter referred to as an Ex. OR circuit) 241. The Ex. OR circuit 241 has a pair of input terminals, which receive a data input signal (D) from the semiconductor integrated circuit device (not shown) and an external expected data signal (EXP) for comparatively checking whether or not the data input signal (D) is normal respectively, figure 1, col. 33, lines 31-32, lines 50-51, lines 53-58, Osawa et al. (i.e. memory module wherein at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from at least one memory component).

- As per claim 39 (method), it follows the same limitations as claim 31 (memory module). Claim 39 is also rejected under the same rationale as set forth in the claim 31 (as rejected above).
- As per claim 40 (method), it follows the same limitations as claim 38 (memory module). Claim 40 is also rejected under the same rationale as set forth in the claim 38 (as rejected above).
- As per claim 41 (method), it follows the same limitations as claim 32 (memory module). Claim 41 is also rejected under the same rationale as set forth in the claim 32 (as rejected above).
- As per claim 42 (method), it follows the same limitations as claim 33 (memory module). Claim 42 is also rejected under the same rationale as set forth in the claim 33 (as rejected above).
- As per claim 45 (method), it follows the same limitations as claim 36 (memory module). Claim 45 is also rejected under the same rationale as set forth in the claim 36 (as rejected above).
- As per claim 47 (method), it follows the same limitations as claim 38 (memory module). Claim 47 is also rejected under the same rationale as set forth in the claim 38 (as rejected above).

17. Claims 34 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 6,415,403 B1), Osawa et al. (US 5,946,247), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1) as applied to claim 31 above, and further in view of Beffa et al. (US 6,058,056). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

18. Claims 35 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 6,415,403 B1), Osawa et al. (US 5,946,247), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1) as applied to claim 31 above, and further in view of Okazaki (US 6,019,501). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

19. Claims 37 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 6,415,403 B1), Osawa et al. (US 5,946,247), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1) as applied to claim 31 above, and further in view of Hii et al. (US 5,883,843). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

20. Claims 48, 49, 50, 51 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 6,415,403 B1) in view of Osawa et al. (US 5,946,247), Beffa et al. (US 6,058,056), Okazaki (US 6,019,501), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1).

As per claim 48, Huang et al. teaches built-in self test for memory (figure 1, col. 4, line 11, Huang et al.), comprising:

At least one memory component (DRAM 13 in figure 1, col. 4, line 13, Huang et al.);

An address and command buffer adapted to transmit address and command data and test data to at least one memory component (interface buffers 14 and DRAM 13 in figure 1, col. 4, lines 14-17, lines 26-29, Huang et al.); and

At least one data buffer to receive the test data from the address and command buffer, to receive the test data from at least one memory component, and to compare the test data received from the address and command buffer with the test data received from at least one memory component to generate the test result (col. 4, lines 14-18, lines 31-33, Huang et al.).

The Examiner would like to point out that the data buffers and the address and command buffer may be incorporated into a single buffer device (page 3, lines 20-21, specification of the present invention).

However Huang et al. do not explicitly teach the specific use of a register to receive a test result. Osawa et al. in an analogous art, teach that the register circuit 706 receives the test result upon the RAM test by the self-test circuit 702 (figure 142, col. 77, lines 62-64, Osawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Osawa et al. by including an additional step of using a register to receive a test result.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a register to receive a test result would provide the opportunity to hold the test result in form of binary data.

Huang et al. do not explicitly teach the specific use of a clock multiplier to receive a clock signal and to multiply the clock signal for transmission.

Beffa et al. in an analogous art, teach a clock multiplier circuit having an input coupled to the external clock terminal, the multiplier circuit developing an internal clock signal on an output in response to the external clock signal, the internal clock signal having a frequency greater than the frequency of the

external clock signal and a control circuit coupled to the output of the clock multiplier circuit and the memory cell arrays (figure 1, col. 9, lines 64-67, col. 10, lines 1-2, lines 35-37, Beffa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Beffa et al. by including an additional step of using a clock multiplier to receive a clock signal and to multiply the clock signal for transmission to the memory component.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a clock multiplier to receive a clock signal and to multiply the clock signal for transmission to the memory component would provide the opportunity to reduce the time and thus the cost of testing the memory component and to conduct the test at the high speeds at which the memory component may operate during use.

Huang et al. do not explicitly teach the specific use of an address and command generator to generate the address and command data.

Okazaki, in an analogous art, teaches that with such an address-generating device according to the first aspect of the invention, it is possible to switch the mode of operation between the address generation and the command generation (col. 5, lines 9-12, Okazaki).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Okazaki by including an additional step of using an address and command generator to generate the address and command data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using an address and command generator to generate the address and command data would provide the opportunity to specify the address of the memory to be tested and to specify mode of operation of the memory under test.

Huang et al. also does not teach a memory module with built-in self-test.

However Cloud et al. in an analogous art teach that the memory device 10 is a SDRAM and the memory module 12 may also include a BIST circuit 73 for testing the circuitry on the module 12 (figure 6, col. 6, lines 12-13, lines 33-34, Cloud et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Cloud et al. by including an additional step of using a memory module with built-in self-test.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a memory module with built-in self-test would provide the opportunity to independently test a memory component without affecting other circuits.

Huang et al. also does not teach that the plurality of memory components, the address and command buffer, and the at least one data buffer all reside within the memory module.

However Ryan in an analogous art teaches that each memory module 320 has at least one pipelined memory subsystem. For purposes of illustration, memory module 320.1 is shown with a single pipelined memory subsystem 330. Memory subsystem 330 comprises C/A buffer register 331, a plurality M of memory devices 335 and a data buffer 341. C/A buffer register 331 is coupled between C/A bus 310 and the plurality M of memory devices 335.1 through 335.M. C/A buffer register 331 receives and latches the command and address information from C/A bus 310. Data register 341 is connected between data bus 315 and the plurality M of memory modules 335. For memory read operations, data register 341 receives and latches data information from the plurality of memory devices 335 and drives the data information to data bus 320. For memory write operations, data register 341 receives and latches data information from data bus 320 and drives the data information to the plurality of memory devices (figure 3, col. 7, lines 29-45, Ryan).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Huang et al.'s patent with the teachings of Ryan by including an additional step of using the plurality of memory components, the address and command buffer, and the at least one data buffer all residing within the memory module.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the plurality of memory components, the address and command buffer, and the at least one data buffer all residing within the memory module would provide the opportunity to provide a memory system with large data storage capacity.

- As per claim 49, Huang et al., Osawa et al., Beffa et al., Okazaki, Cloud et al., and Ryan teach the additional limitations.

Huang et al. teach the memory module wherein the address and command buffer and the data buffer are within a single buffer chip (figure 1, col. 4, lines 10-14, Huang et al.).

- As per claim 50, Huang et al., Osawa et al., Beffa et al., Okazaki, Cloud et al., and Ryan teach the additional limitations.

Huang et al. teach the memory module wherein at least one memory component is a dynamic random access memory, DRAM (DRAM 13 in figure 1, col. 4, lines 13-14, Huang et al.).

- As per claim 51, Huang et al., Osawa et al., Beffa et al., Okazaki, Cloud et al., and Ryan teach the additional limitations.

Osawa et al. teach that the self-test circuit 702 includes a microcomputer 702a as shown in FIG. 143. A program stored in a ROM or a RAM (not shown) of the microcomputer 702a controls a self-test operation. In FIG. 143, a test pattern signal supplied to the RAM with test circuit 703 is indicated as "Test Pattern", figure 142, 143, col. 75, lines 54-57, 67, col. 76, lines 1-2, Osawa et al. (i.e. memory module, wherein the test data is obtained from a data bus through a memory controller).

- As per claim 53, Huang et al., Osawa et al., Beffa et al., Okazaki, Cloud et al., and Ryan teach the additional limitations.

Osawa et al. teach that FIG. 1 is a logic circuit diagram showing a semiconductor memory (RAM) testing device. The comparison circuit 232 is formed by a single exclusive OR circuit (hereinafter referred to as an Ex. OR circuit) 241. The Ex. OR circuit 241 has a pair of input terminals, which receive a data input signal (D) from the semiconductor integrated circuit device (not shown) and an external expected data signal (EXP) for comparatively checking whether or not the data input signal (D) is normal respectively,

figure 1, col. 33, lines 31-32, lines 50-51, lines 53-58, Osawa et al. (i.e. memory module wherein at least one data buffer utilizes an exclusive-OR (XOR) comparator to compare the test data received from the address and command buffer with the test data received from at least one memory component).

21. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 6,415,403 B1), Osawa et al. (US 5,946,247), Beffa et al. (US 6,058,056), Okazaki (US 6,019,501), Cloud et al. (US 5,815,427) and Ryan (US 6,247,070 B1) as applied to claim 48 above, and further in view of Hii et al. (US 5,883,843). See paper no. 7, dated 2/13/03 for detailed action of prior rejections.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Dipakkumar Gandhi
Patent Examiner
June 30, 2003

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